Remote Control Functions

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SELECTOR GUIDE

Function	Number of Address Lines	Maximum Number of Address Codes	Number of Data Bits	Operation	Device Number
Addressable UART	7	128	7/8	Full Duplex	MC14469
Transmitter	0	0	6	Simplex	MC14497
Encoder	Depends on Decoder	Depends on Decoder	Depends on Decoder	Simplex	MC145026
Decoder	5	243	4	Simplex	MC145027
Decoder	9	19,683	0	Simplex	MC145028
Encoder/Decoder	9	512	0	Half Duplex	MC145030
Encoder	13 or 17	131,072	4	Simplex	MC145031 MC145034
Decoder	13 or 17	131,072	4	Simplex	MC145032 MC145035
Encoder/Decoder	15	32,768	0	Half Duplex	MC145033

MC14469

Addressable Asynchronous Receiver/Transmitter

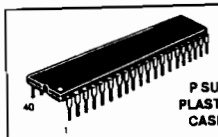
CMOS

The MC14469 receives one or two eleven-bit words in a serial data stream. One of the incoming words contains the address and when the address matches, the MC14469 then transmits information in two eleven-bit-word data streams. Each of the transmitted words contains eight data bits, an even parity bit, and start and stop bits.

The received word contains seven address bits with the address of the MC14469 set on seven pins. Thus 2^7 or 128 units can be interconnected in simplex or full duplex data transmission. In addition to the address received, seven command bits may be received for general-purpose data or control use.

The MC14469 finds application in transmitting data from remote A-to-D converters, remote MPUs, or remote digital transducers to the master computer or MPU.

- Supply Voltage Range: 4.5 V to 18 V
- Low Quiescent Current: 75 µA Maximum @ 5 V, 25°C
- Guaranteed Data Rates to 4800 Baud @ 5 V, to 9600 Baud @ 12 V
- Receive — Serial to Parallel
  Transmit — Parallel to Serial
- Transmit and Receive Simultaneously in Full Duplex
- Crystal or Resonator Operation for On-Chip Oscillator
- See Application Note AN-806A
- Chip Complexity: 1200 FETs or 300 Equivalent Gates



P SUFFIX
PLASTIC DIP
CASE 711

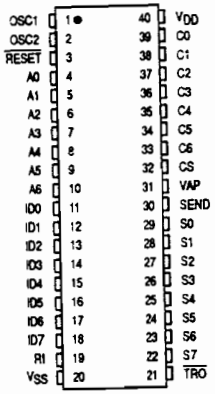
FN SUFFIX
PLCC
CASE 777

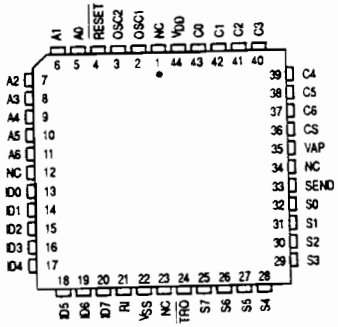
ORDERING INFORMATION

MC14469P	Plastic DIP
MC14469FN	PLCC

6

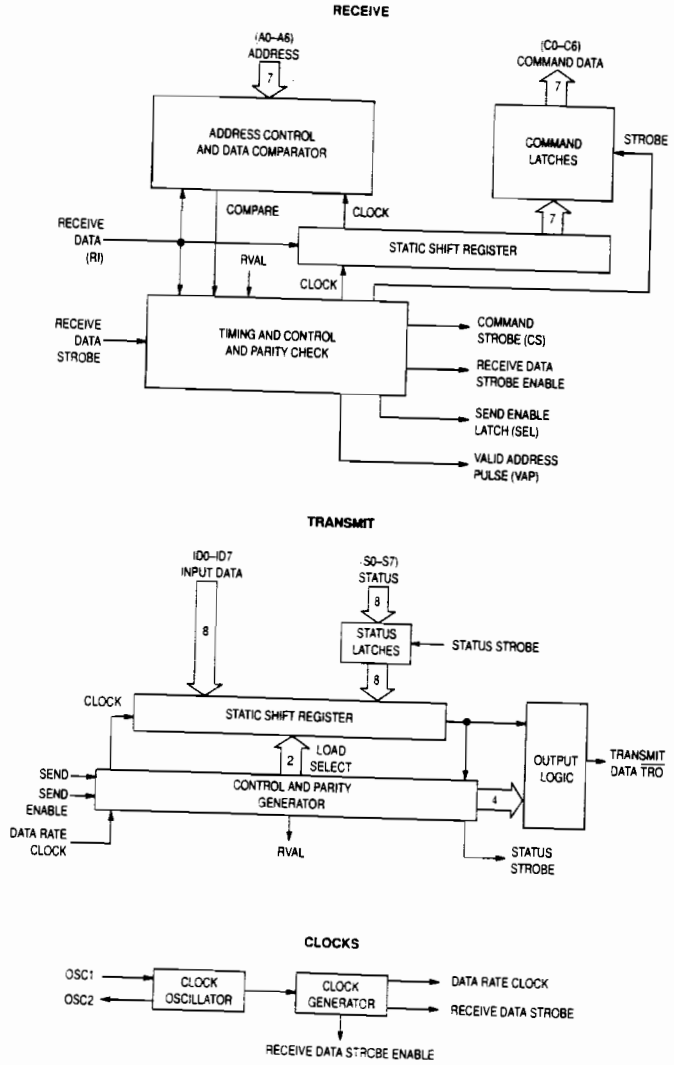
PIN ASSIGNMENTS





NC = NO CONNECTION

BLOCK DIAGRAM



MAXIMUM RATINGS (Voltages referenced to V_{SS})

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +18	V
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD}+0.5	V
DC Current Drain per Pin	I	10	mA
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

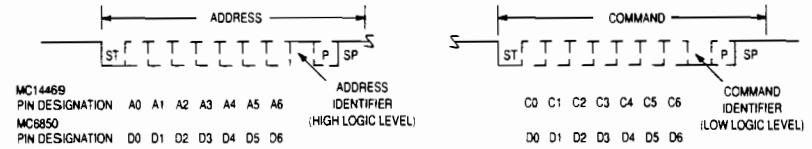
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

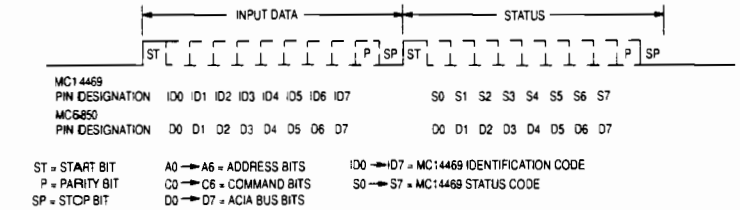
Characteristic		Symbol	V_{DD} V	−40°C Min	−40°C Max	25°C Min	25°C Max	+85°C Min	+85°C Max	Unit
Output Voltage	"0" Level	V_{OL}	5.0	—	0.05	—	0.05	—	0.05	V
V_{in} = V_{DD} or 0			10	—	0.05	—	0.05	—	0.05	
			15	—	0.05	—	0.05	—	0.05	
	"1" Level	V_{OH}	5.0	4.95	—	4.95	—	4.95	—	V
V_{in} = 0 or V_{DD}			10	9.95	—	9.95	—	9.95	—	
			15	14.95	—	14.95	—	14.95	—	
Input Voltage (Except OSC1)	"0" Level	V_{IL}								V
(V_O = 4.5 or 0.5 V)			5.0	—	1.5	—	1.5	—	1.5	
(V_O = 9.0 or 1.0 V)			10	—	3.0	—	3.0	—	3.0	
(V_O = 13.5 or 1.5 V)			15	—	4.0	—	4.0	—	4.0	
	"1" Level	V_{IH}								V
(V_O = 0.5 or 4.5 V)			5.0	3.5	—	3.5	—	3.5	—	
(V_O = 1.0 or 9.0 V)			10	7.0	—	7.0	—	7.0	—	
(V_O = 1.5 or 13.5 V)			15	11	—	11	—	11	—	
Output Drive Current (Except OSC2)		I_{OH}								mA
(V_{OH} = 2.5 V)	Source		5.0	−1.0	—	−0.8	—	−0.6	—	
(V_{OH} = 4.6 V)			5.0	−0.2	—	−0.16	—	−0.12	—	
(V_{OH} = 9.5 V)			10	−0.5	—	−0.4	—	−0.3	—	
(V_{OH} = 13.5 V)			15	−1.4	—	−1.2	—	−1.0	—	
(V_{OL} = 0.4 V)	Sink	I_{OL}	5.0	0.52	—	0.44	—	0.36	—	mA
(V_{OL} = 0.5 V)			10	1.3	—	1.1	—	0.9	—	
(V_{OL} = 1.5 V)			15	3.6	—	3.0	—	2.4	—	
Output Drive Current (OSC2 Only)		I_{OH}								mA
(V_{OH} = 2.5 V)	Source		5.0	−0.19	—	−0.16	—	−0.13	—	
(V_{OH} = 4.6 V)			5.0	−0.04	—	−0.035	—	−0.03	—	
(V_{OH} = 9.5 V)			10	−0.09	—	−0.08	—	−0.06	—	
(V_{OH} = 13.5 V)			15	−0.29	—	−0.27	—	−0.2	—	
(V_{OL} = 0.4 V)	Sink	I_{OL}	5.0	0.1	—	0.085	—	0.07	—	mA
(V_{OL} = 0.5 V)			10	0.17	—	0.14	—	0.1	—	
(V_{OL} = 1.5 V)			15	0.5	—	0.42	—	0.3	—	
OSC Frequency		f_{OSC}	4.5	0	400	0	365	0	310	kHz
			12	0	800	0	730	0	620	
Input Current		I_{in}	15	—	±0.3	—	±0.3	—	±1.0	µA
Pull-Up Current (A0–A6, ID0–ID7)		I_{UP}	15	12	120	10	100	8.0	85	µA
Input Capacitance (V_{in} = 0)		C_{in}	—	—	—	—	7.5	—	—	pF
Quiescent Current (Per Package)		I_{DD}	5.0	—	75	—	75	—	565	µA
			10	—	150	—	150	—	1125	
			15	—	300	—	300	—	2250	
Supply Voltage		V_{DD}	—	+4.5	+18	+4.5	+18	+4.5	+18	V

DATA FORMAT AND CORRESPONDING DATA POSITION AND PINS FOR MC14469 AND MC6850

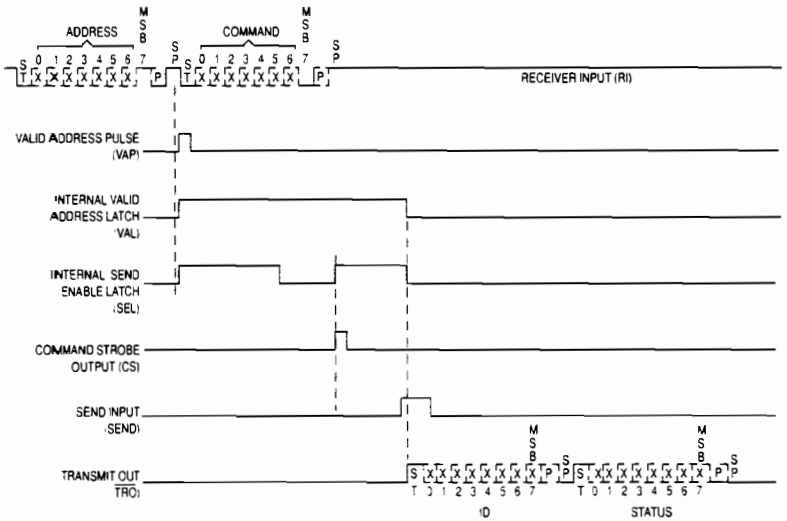
RECEIVE DATA (RI)



TRANSMIT DATA ($\overline{TRO}$)



TYPICAL RECEIVE/SEND CYCLE



PIN DESCRIPTIONS

OSCILLATOR (OSC1, OSC2)

These pins are the oscillator input and output. (See Figure 1.)

RESET ($\overline{RESET}$)

When this pin is pulled low for a minimum of 700 ns, the circuit is reset and ready for operation.

ADDRESS (A0–A6)

These inputs are the address setting pins which contain the address match for the received signal. Pins A0 through A6 have on-chip pullup resistors.

INPUT DATA (ID0–ID7)

These pins contain the input data for the first eight bits of data to be transmitted. Pins ID0–ID7 have on-chip pullup resistors.

RECEIVE INPUT (RI)

This is the receive input pin.

NEGATIVE POWER SUPPLY (VSS)

This pin is the negative power supply connection. Normally this pin is system ground.

TRANSMIT REGISTER OUTPUT SIGNAL ($\overline{TRO}$)

This pin transmits the outgoing signal. Note that it is inverted from the incoming signal. It must go through one stage of inversion if it is to drive another MC14469.

SECOND OR STATUS INPUT DATA (S0–S7)

These pins contain the input data for the second eight bits of data to be transmitted.

SEND (SEND)

This pin accepts the send command after receipt of an address.

VALID ADDRESS PULSE (VAP)

This is the output for the valid address pulse upon receipt of a matched incoming address.

COMMAND STROBE (CS)

This is the output for the command strobe signifying a valid set of command data (C0 through C6).

COMMAND WORD (C0–C6)

These pins are the readout of the general-purpose command word which is the second word of the received signal.

POSITIVE POWER SUPPLY (VDD)

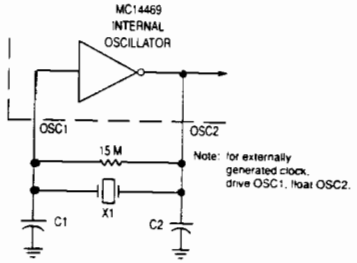
This pin is the package positive power supply pin.

OPERATING CHARACTERISTICS

The receipt of a start bit on the receive input (RI) line causes the receive clock to start at a frequency equal to that of the oscillator divided by 64. All received data is strobed in at the center of a receive clock period. The start bit is followed by eight data bits. Seven of the bits are compared against states of the address of the particular circuit (A0–A6). Address is latched 31 clock cycles after the end of the start bit of the incoming address. The eighth bit signifies an address word "1" or a command word "0". Next, a parity bit is received and checked by the internal logic for even parity. Finally a stop bit is received. At the completion of the cycle if the address matches, a valid address pulse (VAP) occurs. Immediately following the address word, a command word is received. It also contains a start bit, eight data bits, even parity bit, and a stop bit. The eight data bits are composed of a seven-bit command, and a "0" which indicates a command word. At the end of the command word a command strobe pulse (CS) occurs.

A positive transition on the send input initiates the transmit sequence. Send must occur within 7 bit times of CS. Again the transmitted data is made up of two eleven-bit words, i.e., address and command words. The data portion of the first word is made up from input data inputs (ID0–ID7), and the data for the second word from second input data (S0–S7) inputs. The data on inputs ID0–ID7 is latched one clock before the falling edge of the start bit. The data on inputs S0–S7 is latched on the rising edge of the start bit. The transmitted signal is the inversion of the received signal, which allows the use of an inverting amplifier to drive the lines. $\overline{TRO}$ begins either 1 2 or 1-1/2 bit times after send, depending where send occurs.

The oscillator can be crystal controlled or ceramic resonator controlled for required accuracy. OSC1 can be driven from an external oscillator. See Figure 1.



X1 = Ceramic Resonator: 307.2 kHz ± 1 kHz for 4800 baud rate.
C1 and C2 are sized per the ceramic resonator supplier's recommendation.

Ceramic Resonator Suppliers:*
1. Morgan Matroc, Inc., Bedford, OH, 216/232-8600
2. Radio Materials Co., Attica, IN, 317/762-2491

* Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of ceramic resonator suppliers.

Figure 1. Oscillator Circuit

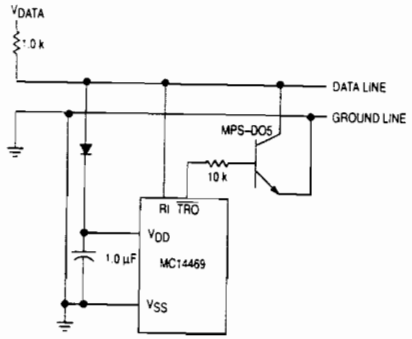


Figure 2. Rectified Power from Data Lines Circuit

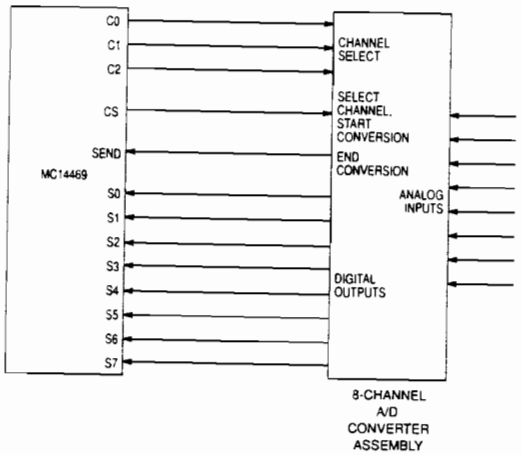


Figure 3. A-D Converter Interface

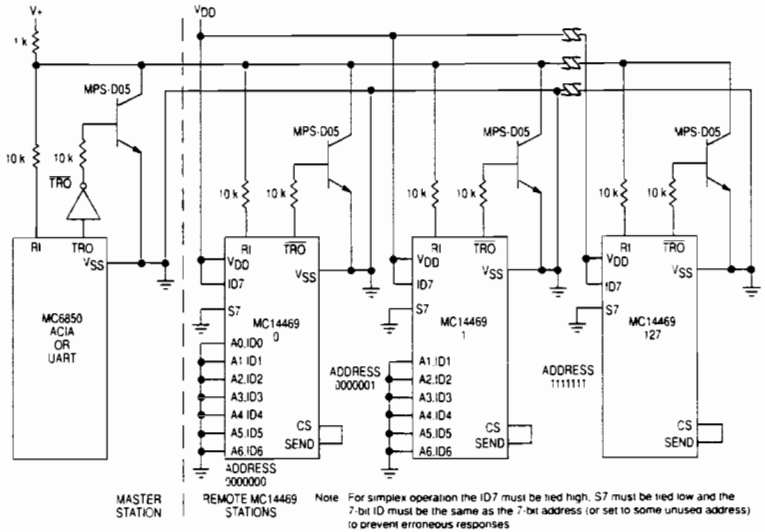


Figure 4. Single Line, Simplex Data Transmission

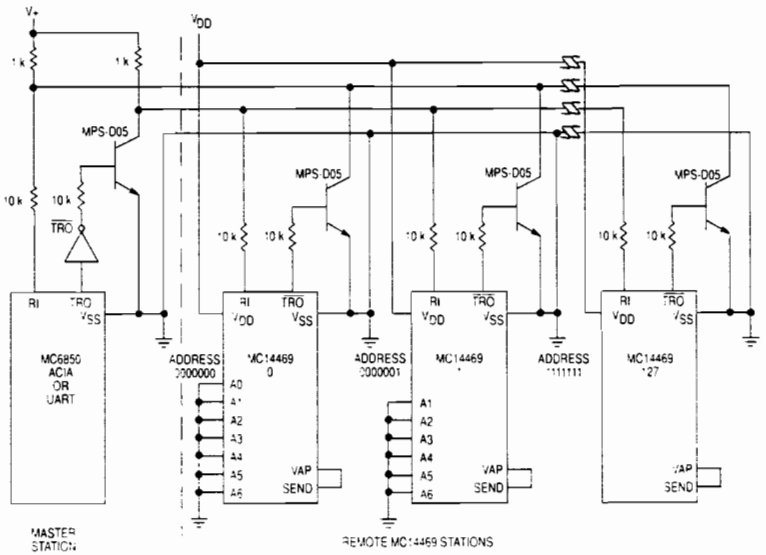


Figure 5. Double Line, Full Duplex Data Transmission

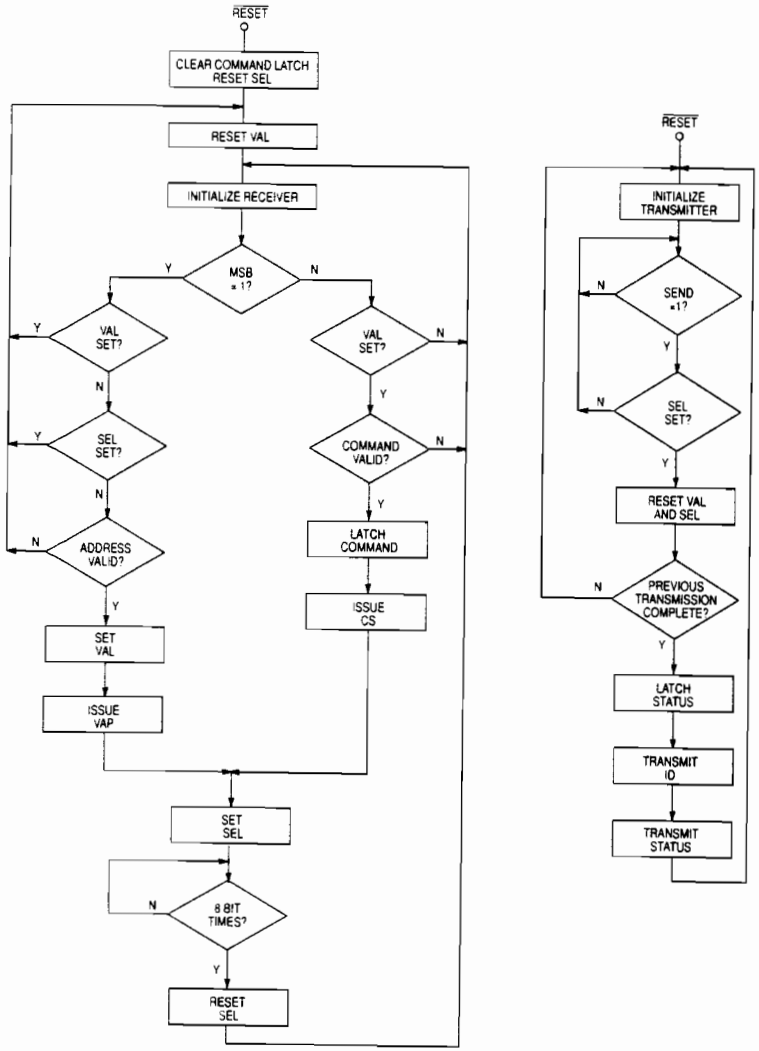


Figure 6. Flow Chart of MC14469 Operation

MC14497

PCM REMOTE CONTROL TRANSMITTER

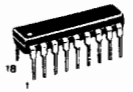
The MC14497 is a PCM remote control transmitter realized in CMOS technology. Using a dual-single (FSK/AM) frequency biphase modulation, the transmitter is designed to work with the MC3373 receiver. Information on the MC3373 can be found in the Motorola *Linear and Interface Integrated Circuits* book (DL128/D).

There is not a decoder device which is compatible with the MC14497. Typically, the decoding resides in MCU software.

- Both FSK/AM Modulation Selectable
- 62 Channels — Up to 62 Keys
- Reference Oscillator Controlled by Inexpensive Ceramic Resonator — Maximum Frequency = 500 kHz
- Very Low Duty Cycle
- Very Low Standby Current: 50 μA Maximum
- Infrared Transmission
- Selectable Start-Bit Polarity (AM only)
- Shifted Key Mode Available
- Wide Operating Voltage Range: 4 to 10 Volts
- See Application Notes AN1016 and AN1203

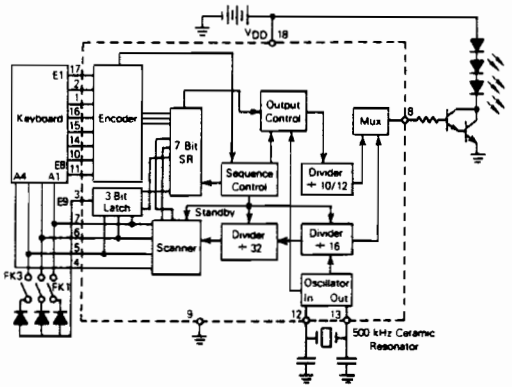
CMOS MSI
(LOW-POWER COMPLEMENTARY MOS)

PCM REMOTE CONTROL TRANSMITTER



P SUFFIX
PLASTIC DIP
CASE 707

FIGURE 1 — BLOCK DIAGRAM



PIN ASSIGNMENT